

DOUBLE GATE TRENCH TRANSISTOR

Abstract of the Disclosure

A field effect transistor is formed with a sub-lithographic conduction channel and a dual gate which is formed by a simple process by starting with a silicon-on-insulator wafer, allowing most etching processes to use the buried oxide as an etch stop. Low resistivity of the gate, source and drain is achieved by silicide sidewalls or liners while low gate to junction capacitance is achieved by recessing the silicide and polysilicon dual gate structure from the source and drain region edges.

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